



Enhancement of electrical characteristics and reliability of CuGeS₂/GeS₂-based super-linear-threshold-switching device by insertion of TiN liner

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Received: 19 April 2022 / Revised: 22 April 2022 / Accepted: 25 April 2022 / Published online: 7 June 2022
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Abstract

For preventing a sneak current in the 3D cross-point array, the selection device is essentially necessary and an n-MOSFET has been used for the selection device. However, the three-terminal electrodes of n-MOSFET make to achieve a high density of a cross-point array difficult. As a solution, using a selector having two terminal electrodes has been intensively researched. We presented that the CuGeS₂/GeS₂-based super-linear-threshold-switching (SLTS) selector device with the insertion of optimal TiN liner thickness exhibited outstanding electrical characteristics and reliability. The dependency of electrical characteristics and reliability on various TiN liner thicknesses were investigated. In addition, the principles of reliability and electrical characteristics improvement were understood through the energy dispersive spectroscopy elemental mapping and line profile of Cu. The adequate amount of Cu distributed in GeS₂ resistive switching layer is a key factor to achieve excellent electrical characteristics and reliability for an ultra-high-density 3D cross-point array cell.

Keywords 3D cross-point array · Super-linear-threshold switching · Selector · GeS₂ · TiN liner · Endurance cycle

1 Introduction

Recently, the demand for large data storage and fast processing has rapidly increased for the big data markets such as artificial intelligence (AI), virtual reality (VR), autonomous car, and the internet of things (IoT). Thus, a new concept of the memory, storage-class memory (SCM), has been introduced since it exhibited a higher bit density and 1,000 times faster-switching speed than the conventional NAND flash memory [1]. In general, SCM has been fabricated with three-dimensional (3D) cross-point memory cell array for ultrahigh-density memory applications [2, 3]. Typically, 3D cross-point memory cell array based on the single resistor (1R) such as phase-change-random-access-memory (PCRAM), resistive-random-access-memory (ReRAM), and p-spin-torque-transfer-random-access-memory

(p-STTMRAM), suffers from the leakage current of the unselected memory cells which would hinder the device operation in large scale. The configuration in which a selector (1S) is stacked vertically with a resistor (1R) has been proposed to eliminate the leakage current [4]. The selector device should have ultralow leakage current (i.e., ~ 1 pA) and high selectivity (i.e., ~ 10⁷) to avoid any undesired operation of the unselected memory cells. Previous work has reported a number of selectors including ovonic threshold switch (OTS) [5, 6], insulator–metal transition (IMT) [7, 8], field-assisted super-linear threshold (FAST) [9], and mixed ionic–electronic conduction (MIEC) [10, 11]. Among the various types of selector device, mixed-ionic-electronic-conduction (MIEC) type selector has been intensively researched as it exhibited an abrupt threshold switching through the formation and rupture of the metal filaments, resulting in high selectivity (i.e., ~ 10⁴) and low leakage current (i.e., ~ 10 pA). However, the selector device using metal filaments suffers from reliability issues such as poor endurance due to the accumulation of excessive amounts of metal ions in the switching layer [12–14]. Therefore, it is important to find an efficient solution that improves selectivity and endurance characteristics by controlling the diffusion of excessive amounts of metal ions.

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In this study, MIEC type Cu-doped GeS₂ (CuGeS₂)/GeS₂-based super-linear-threshold-switching (SLTS) selector using an optimal TiN liner thickness could improve the electrical characteristics and reliability. Our proposed SLTS device utilized GeS₂ as the switching layer and CuGeS₂ as the ion supply layer. GeS₂ has a relatively large bandgap compared to other chalcogenide materials, which is advantageous for achieving low off current and high selectivity [15]. Furthermore, the CuGeS₂ was applied as an ion supply layer instead of Cu which would reduce the stability of the Cu filament so that the volatile properties would be maintained better [16]. The dependency of the TiN liner thickness on the reliability and electrical characteristics (i.e., V_{th} , V_h , selectivity) of the CuGeS₂/GeS₂-based SLTS selector device were investigated to determine the optimal TiN liner thickness. Furthermore, the effects of TiN liner thickness on Cu diffusion were assessed in detail using transmission electron microscopy (TEM), energy dispersive spectroscopy (EDS) elemental mapping, and line profile.

2 Experiments and discussion

A SiO₂ film was deposited by chemical vapor deposition (CVD) on a wafer with a structure of Si/SiO₂/W/SiN_x, where cylindrical-shaped holes with 218 nm were patterned by photolithography and dry etching. W bottom electrodes were deposited with ~50 nm thickness, followed by chemical mechanical planarization (CMP). The photolithography process was proceeded with 60 × 60 μm² square pattern. Then, ~5-nm-thick GeS₂ layer was deposited by RF magnetron sputtering at 40 W RF power, 40 sccm Ar flow rate using a GeS₂ alloy target. Afterwards, TiN liner with 0 to 2 nm thickness was deposited by DC magnetron sputtering at 20 W DC power, 30 sccm Ar flow rate using a TiN alloy target. CuGeS₂ layer with ~5 nm thickness was deposited by RF magnetron co-sputtering technique using Cu and GeS₂

targets in the condition of Ar flow rate of 40 sccm, and working pressure of 4 × 10⁻³ Torr. A top Pt electrode was deposited by DC magnetron sputtering at DC power of 30 W, Ar flow rate of 30 sccm, and working pressure of 2 × 10⁻³ Torr using a Pt target. Thus, after the lift-off process, the CuGeS₂/GeS₂-based SLTS selector cells were fabricated with a vertical structure of the bottom W electrode with a diameter of 218 nm, GeS₂ resistive switching layer, TiN liner, CuGeS₂ ion supply layer, and top Pt electrode. The material properties of the GeS₂ resistive switching layer were observed by X-ray diffraction, X-ray photoelectron spectroscopy, and UV–vis spectrophotometer. The electrical properties were measured using Agilent B2902A semiconductor and Keithley 4200A-SCS parameter analyzers. The effects of TiN liner thickness on Cu diffusion were analyzed by using transmission electron microscopy (TEM), energy dispersive spectroscopy (EDS) elemental mapping, and line profile.

To design the unstable Cu-filament-based SLTS selector device, GeS₂ and CuGeS₂ were utilized as the resistive switching layer and ion supply layer, respectively. Since the GeS₂ resistive switching layer, which has a relatively high energy bandgap compared to conventional chalcogenide material (i.e., GeTe₆ ~ 0.6 eV, GeSe ~ 1.0 eV) [17, 18], it is beneficial for achieving low off current and therefore larger selectivity. In addition, the CuGeS₂ layer serves as a Cu ion supply layer for forming the unstable Cu filaments in the GeS₂ layer. The material properties of the GeS₂ layer were investigated using X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and UV–vis spectrophotometer (UV–vis), as shown in Fig. 1. Through the XRD analysis, the crystalline characteristics of the GeS₂ were confirmed depending on the N₂ post-annealing temperature (as-sputtered, 100, 200, 300, and 400 °C), as shown in Fig. 1a. Since a high resistance is essential to obtain a low off-state current, an amorphous GeS₂ without an annealing process was selected as the resistive switching layer. Note that further annealing above 100 °C would transform the

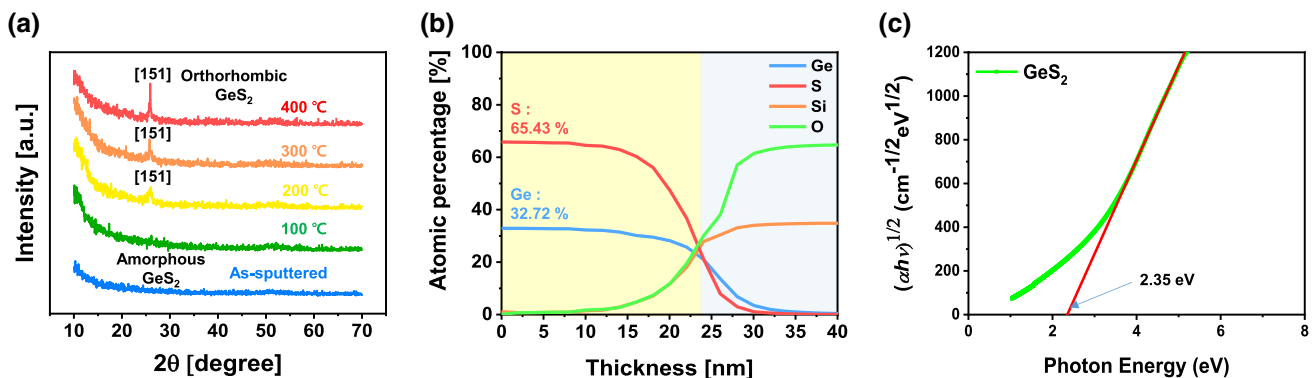


Fig. 1 Material properties of GeS₂ resistive switching layer. **a** Dependency of crystallinity of GeS₂ resistive switching layer on N₂ post-annealing temperature, **b** chemical compositional depth profiles, and **c** tauc plots of calculating the energy band gap of GeS₂ resistive switching layer

crystallinity of the GeS_2 resistive switching layer from an amorphous to an orthorhombic structure [19], which may lower the resistance. In addition, the chemical composition of the GeS_2 resistive switching layer was observed using the XPS chemical depth profile. The composition ratio of Ge and S were ~ 65.43 and ~ 32.72 , as shown in Fig. 1b. The energy bandgap of amorphous GeS_2 was determined to be 2.35 eV by linear fitting of the near absorption edge in the Tauc plot, $(\alpha h\nu)^{1/2}$ as a function of photon energy $h\nu$ displayed in Fig. 1c, where α is the absorption coefficient. These results indicate how GeS_2 -based SLTS selector device could exhibit outstanding device performance such as low off current. Furthermore, to achieve the high current and high selectivity, the CuGeS_2 ion supply layer was used to form the Cu-filament. However, the selector device operated by the formation and rupture of the metal filaments suffer from poor endurance due to the accumulation of excessive amounts of metal ions in the switching layer. Employing a TiN liner would enhance the endurance cycles of the selector device using metal filaments.

To find out the optimal TiN liner thickness, the current (I)- vs. voltage (V) characteristics of the SLTS selector device with the insertion of 0 to 2 nm-thick TiN liner was compared, as shown in Fig. 2a–c. The Cu-filament-based SLTS selector device showed volatile threshold switching current (I)- vs. voltage (V) characteristics when positive bias was applied to the top Pt electrode. As shown in Fig. 2a, in

the case of the SLTS selector device without TiN liner, the current abruptly reached from high resistance state (HRS) to low resistance state (LRS) at a threshold voltage (V_{th}) of ~ 0.60 V, reaching a compliance level of $\sim 5 \times 10^{-5}$ A when a positive bias was applied from 0 to 2.00 V. This result suggested that the Cu filaments were formed between CuGeS_2 ion supply layer and bottom W electrode. As the voltage was swept from 2.00 to 0 V, the device exhibited a holding voltage (V_h) of ~ 0 V and a selectivity of $\sim 4.59 \times 10^5$, reaching the off current of ~ 100 pA. This result implied that the rupture process of Cu-filament spontaneously proceeded, exhibiting typical threshold switching behavior. In the case of the SLTS selector device with 1-nm thick TiN liner, it exhibited a threshold voltage (V_{th}) of ~ 0.85 V, reaching a compliance level of $\sim 5 \times 10^{-5}$ A when a positive bias was applied from 0 to 2.00 V. In addition, as the voltage was swept from 2.00 to 0 V, the device exhibited a holding voltage of ~ 0.10 V and a selectivity of $\sim 8.06 \times 10^5$, reaching the off current of ~ 50 pA. Lastly, in the case of the SLTS selector device with 2-nm thick TiN liner, it exhibited a threshold voltage (V_{th}) of ~ 1.00 V, reaching a compliance level of $\sim 5 \times 10^{-5}$ A when a positive bias was applied from 0 to 2.00 V. In addition, as the voltage was swept from 2.00 to 0 V, the device exhibited a holding voltage of ~ 0.20 V and a selectivity of $\sim 3.10 \times 10^6$, reaching the off current of ~ 10 pA. The SLTS selector device with TiN liner shows an increased threshold voltage (V_{th}), holding voltage (V_h), and selectivity compared

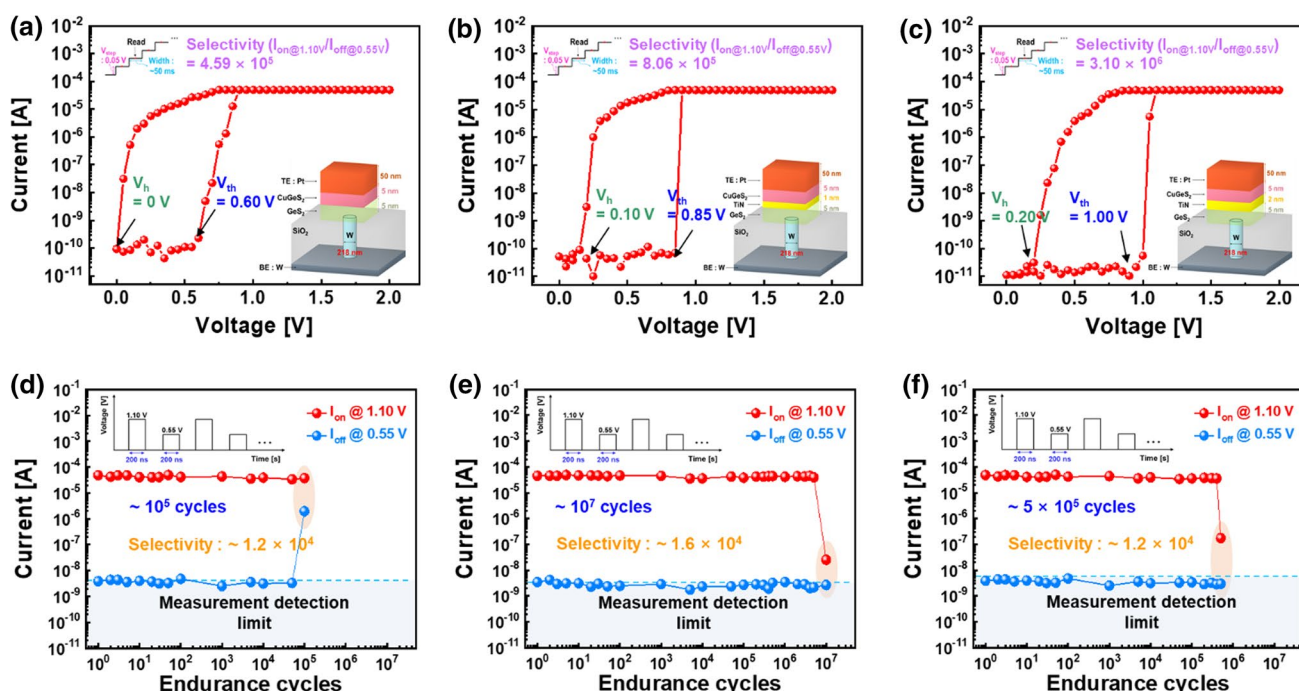


Fig. 2 Dependency of electrical characteristics and reliability of SLTS selector device on TiN liner thickness varying from 0 to 2 nm. DC I-V curve of the selector device with **a** 0-, **b** 1-, and **c** 2-nm-thick

TiN liner, respectively. The endurance cycles of the selector device with **a** 0-, **b** 1-, and **c** 2-nm-thick TiN liner

to the SLTS selector device without TiN liner. This result evidently indicated that the inserted TiN liner hinders the diffusion of Cu from the ion supply layer to the GeS₂ resistive switching layer. The dependency of reliability (i.e., endurance cycles) on the inserted TiN liner thickness was investigated to determine the optimal TiN liner thickness, as shown in Fig. 2d–f. The SLTS selector device without TiN liner demonstrated set-stuck failure (i.e., remaining stuck in the ON-state) after $\sim 10^5$ cycles, as shown in Fig. 2d. During repeated endurance cycles, a continuous accumulation of Cu led to an increase in filament size, preventing spontaneous dissolution. On the contrary, the SLTS selector device with a 1-nm TiN liner demonstrated reset-stuck failure (stuck in the OFF-state) after $\sim 10^7$ cycles, as shown in Fig. 2e. The SLTS selector device with a 2-nm TiN liner demonstrated reset-stuck failure (stuck in the OFF-state) after $\sim 5 \times 10^5$ cycles, as shown in Fig. 2f. This failure may be attributed to a lack of Cu sources during repeated endurance cycles, which would produce relatively thin filament in the GeS₂ resistive switching layer. These results suggested that an optimal TiN liner thickness controlling the diffusion of an appropriate amount of Cu is important for achieving electrically reliable threshold switching characteristics.

The effects of TiN liner on Cu diffusion were directly confirmed using TEM image, EDS elemental mapping and line profiles of Cu, as shown in Fig. 3. As shown in Fig. 3a, the SLTS device without a TiN liner had Cu source distributed over the entire resistive switching layer, resulting in poor reliability. As shown in Fig. 3b, as the thickness of the TiN liner increased from 0 to 1 nm, the integrated area of Cu concentration in the CuGeS₂ ion supply layer was increased from 78.58 to 98.16, while the integrated area of Cu concentration in the GeS₂ resistive switching layer was decreased from 72.26 to 52.04. As shown in Fig. 3c, as the thickness of the TiN liner increased from 1 to 2 nm, the integrated area of Cu concentration in the CuGeS₂ ion supply layer was increased from 98.16 to 116.39, while the integrated area of Cu concentration in the GeS₂ resistive switching layer

was decreased from 52.04 to 34.47. These results evidently indicate that the thickness of the TiN liner determines the amount of Cu in the GeS₂ switching layer. Thus, an adequate amount of Cu distributed in the GeS₂ resistive switching layer is a key factor to achieve outstanding electrical characteristics and reliability.

The schematic illustration of the proposed filament models of the SLTS selector device with various TiN liner thickness was displayed, as shown in Fig. 4. In the case of the SLTS selector device without TiN liner, an excessive amount (i.e., integrated area of ~ 72.26) of Cu sources was observed in the GeS₂ resistive switching layer, which makes the Cu filament thick and difficult to rupture, resulting in set stuck failure, as shown in Fig. 4a. In the case of the SLTS selector device with 1-nm-thick TiN liner, an adequate amount (i.e., integrated area of ~ 52.04) of Cu sources was observed in the GeS₂ resistive switching layer, which makes the Cu filament thinner than the device without TiN liner, as shown in Fig. 4b. As a result, it exhibited the most stable endurance cycles (i.e., $\sim 10^7$). Lastly, in the case of the SLTS selector device with 2-nm-thick TiN liner, an insufficient amount (i.e., integrated area of ~ 34.47) of Cu sources was observed in the GeS₂ resistive switching layer, which makes the Cu filament extremely thin and unstable, as shown in Fig. 4c. This filament model demonstrated that the thickness of the TiN liner determines the amount of Cu diffusion in the GeS₂ resistive switching layer, which either improves or degrades the reliability and electrical characteristics of the SLTS selector device.

3 Conclusion

In summary, we proposed CuGeS₂/GeS₂-based SLTS selector device adopting TiN liner as a diffusion barrier to control the excessive amount of diffusion of Cu into the resistive switching layer, and investigated the effect of TiN liner thickness on electrical characteristics and reliability of SLTS

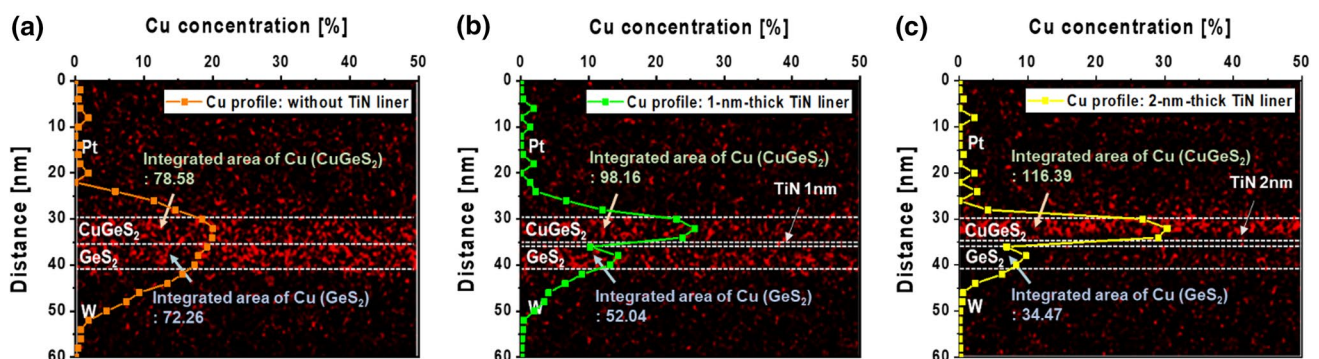
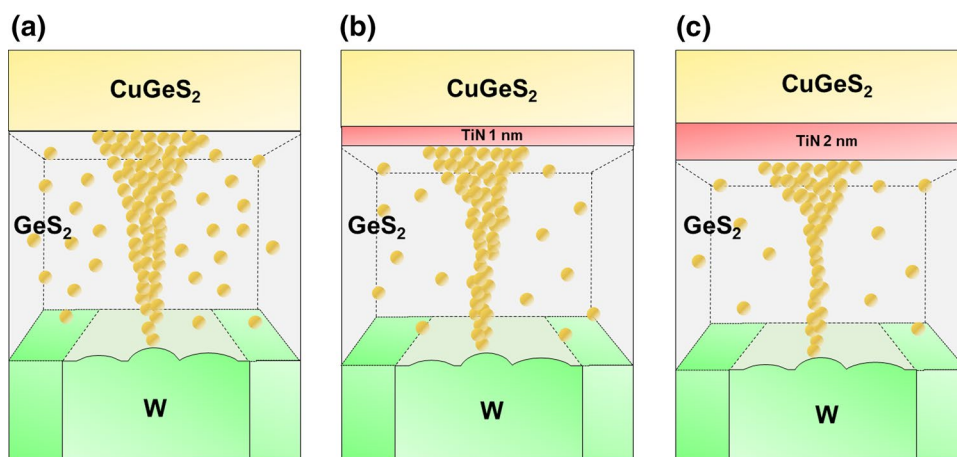


Fig. 3 Dependency of Cu distribution on various TiN liner thickness in SLTS selector device. EDS elemental mapping and line profiles of Cu in SLTS selector device with **a** 0-, **b** 1-, and **c** 2-nm-thick TiN liner

Fig. 4 The schematic illustration of filament formation on TiN liner thickness. The formation of Cu filament in SLTS selector device with **a** 0-, **b** 1-, and **c** 2-nm-thick TiN liner



selector device. As the thickness of TiN liner increased from 0 to 2 nm, the selector device exhibited an increased threshold voltage (V_{th}), holding voltage (V_h) and selectivity which implied that the inserted TiN liner suppressed the diffusion of Cu from the CuGeS_2 ion supply layer. Furthermore, as the thickness of TiN liner increased from 0 to 1 nm, the endurance cycles enhanced from $\sim 10^5$ to $\sim 10^7$. However, as the thickness of TiN liner increased from 1 to 2 nm, the endurance cycles degraded from $\sim 10^7$ to $\sim 5 \times 10^5$. The outstanding endurance cycles (i.e., $\sim 10^7$), low off current (i.e., ~ 50 pA) and selectivity (i.e., $\sim 8.06 \times 10^5$) were achieved by optimizing TiN liner thickness. In addition, the filament model of SLTS selector device with various TiN liner thickness was suggested based on the result of EDS elemental mapping and line profile of Cu. It evidently demonstrated that the thickness of TiN liner determines the amount of Cu diffused into GeS_2 resistive switching layer. This work provides key insights for designing the selector device with outstanding reliability and electrical characteristics for 3D cross-point array cells applied to SCM.

Acknowledgements This research was supported by National R&D Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Science and ICT(2021M3F3A2A01037733).

References

1. S.W. Fong, C.M. Neumann, H.S.P. Wong, IEEE Trans. Electron Devices. **64**, 11 (2017)
2. H.Y. Cheng, F. Carta, W.C. Chien, H.L. Lung, M.J. Brightsky, J. Phys. D Appl. Phys. **52**, 47 (2019)
3. W. C. Chien et al., in Digest of Technical Papers - Symposium on VLSI Technology, pp. T60–61, (2019).
4. G.W. Burr et al., J. Vac. Sci. Technol. B. **32**, 4 (2014)
5. J. Yoo et al., Adv. Electron. Mater. **5**, 7 (2019)
6. Y. Koo, H. Hwang, Sci. Rep. **8**, 1 (2018)
7. D. S. Jeon, T. D. Dongale, and T. G. Kim, J. Alloys Compd., **884**, (2021).
8. D. Chen et al., Ceram. Int. **47**, 16 (2021)
9. S. H. Jo, T. Kumar, S. Narayanan, W. D. Lu, and H. Nazarian, in Technical Digest - International Electron Devices Meeting, IEDM, pp. 6.7.1–6.7.4, (2015).
10. R.S. Shenoy et al., Semicond. Sci. Technol. **29**, 10 (2014)
11. P. Narayanan et al., in Device Research Conference - Conference Digest, DRC, pp. 239–240, (2014).
12. B. Grisafe, M. Jerry, J.A. Smith, S. Datta, IEEE Electron Device Lett. **40**(10), 1602–1605 (2019)
13. X. Zhao et al., Adv. Mater. **30**, 14 (2018)
14. J. Song et al., IEEE Trans. Electron Devices **64**(11), 4763–4767 (2017)
15. S. Jia et al., Nat. Commun. **11**, 1 (2020)
16. Q. Lin et al., IEEE Electron Device Lett. **39**(4), 496–499 (2018)
17. D.M. Guzman, A. Strachan, Phys. Rev. Mater. **1**, 5 (2017)
18. B. Govoreanu et al., in Digest of Technical Papers - Symposium on VLSI Technology, pp. T92–T93, (2017).
19. Y.J. Cho et al., Chem. Commun. **49**(41), 4661–4663 (2013)

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