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ORIGINAL PAPER - CONDENSED MATTER

# Synaptic variation reduction via embedding Au nanocrystals in resistive switching layer and bottom electrode interface for CuTe/CuO/TiN-stacked synaptic device

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**Abstract**
Reliable artificial synaptic devices are essential for the stable and fast training of artificial neural networks (ANNs). Specifically, synaptic devices should be robust during the training and testing of ANNs to embed them in the hyper-scale synaptic cores of neuromorphic computing architectures. In this study, a highly reliable artificial synaptic device based on a CuTe/CuO/TiN-stacked conductive-bridge random-access memory cell having forming-free property was developed via embedding Au nanocrystals in the CuO resistive switching layer and TiN bottom electrode interface. Forming-free property was achieved by precisely designing the diameter of Au nanocrystals implementing the interface between the CuO resistive switching layer and TiN bottom electrode. In particular, this synaptic device exhibited multilevel current states when the compliance current level was varied. In addition, the synaptic device embedding Au nanocrystals (i.e., ~ 17.7 nm in diameter) showed a remarkable reduction of the variation in synaptic modulation. Furthermore, the test accuracy of image recognition via a deep neural network simulation was dramatically improved up to 91.95% using practical synaptic modulation data of the synaptic device embedding Au nanocrystals (i.e., ~ 17.7 nm in diameter).

**Keywords** Conductive-bridge random-access-memory (CBRAM) · Synaptic device · Au nanocrystals · Synaptic variation · Deep neural networks

## 1 Introduction

Memristive devices such as resistive random access memory (ReRAM), phase-change random access memory (PCRAM), ferroelectric random access memory (FeRAM), and memtransistor are promising candidates for artificial synaptic devices with synaptic cores in advanced neuromorphic chips [1–14]. Among these, ReRAM is currently being actively researched as an artificial synaptic device because of its multilevel capability (> 11 bits) [15], high switching speed (< 100 ps) [16], high endurance (> $10^{12}$ cycles) [17], low power consumption (~ 1 mW), high scalability, and complementary metal–oxide–semiconductor (CMOS) compatibility [18]. ReRAM is generally categorized as valence change memory (VCM) with oxygen vacancy filaments and electrochemical metallization cells (ECM) with conductive metal filaments. In particular, ECM (or conductive-bridge random access memory (CBRAM)) cells have the advantage of being able to operate at a lower voltage than VCM owing to the high mobility of metal ions in the oxide-based or chalcogenide-based resistive switching layer [19]. The CBRAM cell consists of a simple metal–insulator-metal (MIM) stack with an active top electrode layer (i.e., Cu, Ag, and CuTe), which is the source of a conductive metal filament, a resistive switching layer, and a bottom electrode (i.e., Pt and TiN). When a positive voltage is applied to the active top electrode layer, Cu or Ag in the active source layer are ionized (i.e., oxidized) such that diffusion and drift occur towards the bottom electrode due to the electric field. Subsequently, Cu or Ag ions are reduced by the supplied electrons at the bottom electrode, and Cu or Ag-based conductive metal filaments are formed in the resistive switching layer. Thereby, CBRAM cells can perform bistable resistance switching by electroforming and rupture dynamics of a conductive metal filament in the resistive switching layer

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using redox processes (i.e., reduction and oxidation) [20, 21].

However, CBRAM cells require an electroforming process for continuous bistable resistive switching, which adversely affects the reliability of the device because it artificially causes the breakdown of the resistive switching layer in the beginning [22–27]. Thus, the reliability of CBRAM cells can be improved by achieving forming-free characteristics. In addition, the electroforming process consumes high power and requires an additional circuit to generate a voltage higher than a set voltage [19]. Moreover, the variation in synaptic modulation would be drastically reduced when applied as an artificial synaptic device due to improvement in the reliability of the CBRAM cell. To date, various studies have been conducted to improve reliability by achieving forming-free characteristics in CBRAM cells [28–30]. However, studies presenting improved recognition performance by forming-free characteristics in neuromorphic applications (i.e., training and testing of deep neural networks (DNN)) have not been conducted.

In this study, we have designed a highly reliable artificial synaptic device based on a CBRAM cell having forming-free characteristics with a TiN capping layer, CuTe active source layer, CuO resistive switching layer embedded with Au nanocrystals (NCs), and a TiN bottom electrode. Forming-free property was achieved by precisely controlling the diameter of the Au NCs embedded in the CuO resistive switching layer. In addition, the variation in synaptic modulation (i.e., long-term potentiation (LTP) and long-term depression (LTD)) was dramatically improved from 20.61 to 1.95%. Finally, a hardware-based DNN simulation with synaptic variations was performed to evaluate the accuracy of the image recognition task.

## 2 Experiments and discussion

In general, in a resistive switching layer, conductive metal filaments are generated stochastically at randomly distributed hillocks on the bottom electrode by a strong electric field applied in the vertical direction [20, 21]. In other words, the stochastic nature of the formation of conductive metal filaments in a resistive switching layer is removed due to the intentionally generated hillock-like surface topography. Thus, in this study, a resistive switching layer embedded with Au NCs was intentionally employed to modulate the surface topography of the TiN bottom electrode and achieve highly reliable synaptic modulation by obtaining forming-free characteristics, as shown in Fig. 1a. The highly reliable CBRAM-based artificial synaptic device was designed

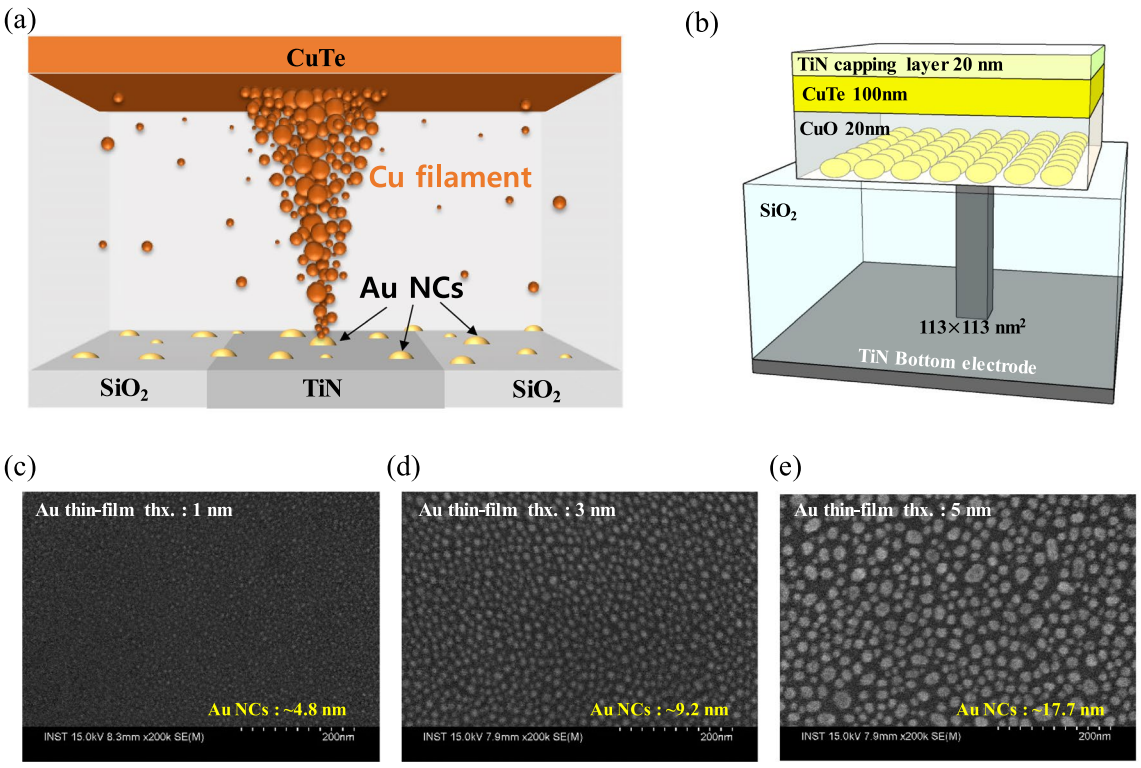


**Fig. 1** CuTe/CuO/TiN-stacked CBRAM cell embedded with Au NCs. **a** Design of the highly reliable CBRAM cell embedded with Au NCs between the CuO resistive switching layer and TiN bottom electrode, **b** device structure of the CBRAM cell, **c–e** top view SEM images of the Au thin films of thicknesses 1, 3, and 5 nm, respectively

with a 20 nm thick TiN capping layer, a 100 nm thick CuTe active source layer, a 20 nm thick CuO resistive switching layer embedded with Au NCs, and a plug-type TiN bottom electrode of area $113 \times 113$ nm$^2$, as shown in Fig. 1b. To embed Au NCs in the CuO resistive switching layer, an Au thin film was deposited on the TiN bottom electrode and post-deposition annealing (PDA) was conducted in a nitrogen atmosphere of 400 °C. Subsequently, the CuO resistive switching layer, CuTe active source layer, and TiN capping layer were sequentially sputtered on the Au NCs after a typical positive photolithography process with a patterning area of $60 \times 60$ μm$^2$. Finally, the CBRAM cells were fabricated by a lift-off process using acetone, methanol, and deionized water. In particular, CuO material was used as the resistive switching layer because Cu-based materials have high thermal stability, natural abundance, nontoxicity, and can be integrated with modern CMOS circuits [30]. To investigate the diameter of Au NCs, Au thin films of thickness 1, 3, and 5 nm were evaporated on the TiN surface sputtered on the $SiO_2$ substrate, and PDA was performed in a nitrogen atmosphere at 400 °C. From scanning electron microscopy (SEM) of the 1 nm thick Au thin film processed by PDA, the average diameter of Au NCs is observed to be ~ 4.8 nm, as shown in Fig. 1c, in which the scale bar size is 200 nm. In the 3- and 5-nm thick Au thin films processed by PDA, the average diameters of Au NCs are ~ 9.2 nm and ~ 17.7 nm, respectively, as shown in Fig. 1d, e. It is inferred that the average diameter of the Au NCs increases with the thickness of the Au thin film. Thus, the average diameter of the Au NCs depends on the thickness of the Au thin film. In addition, unlike the Au NCs in the 1- and 3-nm thick Au thin films, the Au NCs in the 5 nm thick Au thin film appear to be island-shaped on the TiN surface. These island-shaped Au NCs act as hillocks on the TiN bottom electrode and eliminate synaptic variations through forming-free characteristics. To further investigate the height of the Au NCs, four CBRAM devices were fabricated by varying the thickness of the Au thin film in the CuO resistive switching layer, and a cross-sectional transmission electron microscopy (x-TEM) analysis was conducted, as shown in Fig. 2. Unlike in Fig. 2a, the Au NCs in the 1-nm thick Au thin film are located between the CuO resistive switching layer and TiN bottom electrode contact (BEC), as shown in Fig. 2b. Here, the average height of the Au NCs is ~ 3.03 nm, as shown in the magnified inset of Fig. 2b. In the Au thin films of thickness 3 and 5 nm, the average heights of the Au NCs are ~ 5.78 nm and ~ 6.97 nm, respectively, as shown in the magnified insets of Fig. 2c, d. Similar to the trends of the average diameter, the average height of the Au NCs increases linearly with the thickness of the Au thin film. In addition, the electroforming voltage would be decreased with increasing height of the Au NCs and acts as a virtual electrode because of the strong electric field applied in the vertical direction.

To demonstrate the effect of the embedded Au NCs in the CuO resistive switching layer and TiN bottom electrode interface, the electroforming process of the designed CBRAM-based artificial synaptic device was performed by applying DC voltage sweeps at the TiN capping layer. The TiN bottom electrode was grounded during the DC I-V measurements. When the DC voltage was scanned from 0 to 5 V, the CBRAM cell without Au NCs was switched from a high-resistance state (HRS) to a low-resistance state (LRS) with a high electroforming voltage of 3.8 V, as indicated by the blue line in Fig. 3a. This result indicates that conductive Cu filaments were generated in the CuO resistive switching layer owing to the diffusion and drift of Cu ions by the applied electric field. In other words, an almost hard breakdown of the CuO resistive switching layer occurred during the electroforming process. This electroforming process with a high voltage amplitude can adversely affect the reliability of the CBRAM cell. As the thickness of the Au thin film located at the interface of the CuO resistive switching layer and TiN bottom electrode increases from 1 to 5 nm at intervals of 2 nm, the electroforming voltage dramatically decreases from 2.2 to 0.3 V, as shown by the red, orange, and green curves in Fig. 3a. These results demonstrate that the Au NCs inserted at the interface of the CuO resistive switching layer and TiN bottom electrode can reduce the electroforming voltage from 3.8 to 0.3 V. In addition, we expect an improvement in the reliability of the synaptic modulation (i.e., LTP and LTD) in the designed CBRAM-based artificial synaptic device with a decrease in the amplitude of the electroforming voltage. After the electroforming process, bistable resistive switching was conducted by double scanning the DC voltage from 0 to 2 V (i.e., the set region), and from 0 to − 1 V (i.e., the reset region), as shown in Fig. 3b. When the DC voltage was scanned from 0 to 2 V, the CBRAM cell without Au NCs changed from HRS to LRS at 0.76 V, as shown by the blue curve in Fig. 3b. For Au thin films of 1, 3, and 5 nm thickness, the CBRAM cells were switched from HRS to LRS at 0.70 V, 0.52 V, and 0.30 V, respectively, as shown in the red, orange, and green curves in Fig. 3b. All CBRAM cells were changed from LRS to HRS by applying a negative voltage of − 1.2 V with typical negative differential resistance (NDR) phenomena at approximately − 0.1 V. As summarized in Fig. 3c, the forming voltage is decreased from 3.80 to 0.30 V and the set voltage is reduced from 0.76 to 0.30 V. However, the HRS current at 0.2 V is increased from $1.7 \times 10^{-8}$ to $9.3 \times 10^{-7}$ A as the diameter of the Au NCs increases. This tendency is associated with the strengthening of the electric field applied in the vertical direction because the enlarged Au NCs act as virtual electrodes. However, the CBRAM cell embedded with an Au thin film of 5-nm thickness having a set voltage of 0.3 V is the same as the electroforming voltage of 0.3 V, such that forming-free characteristics are achieved. Through

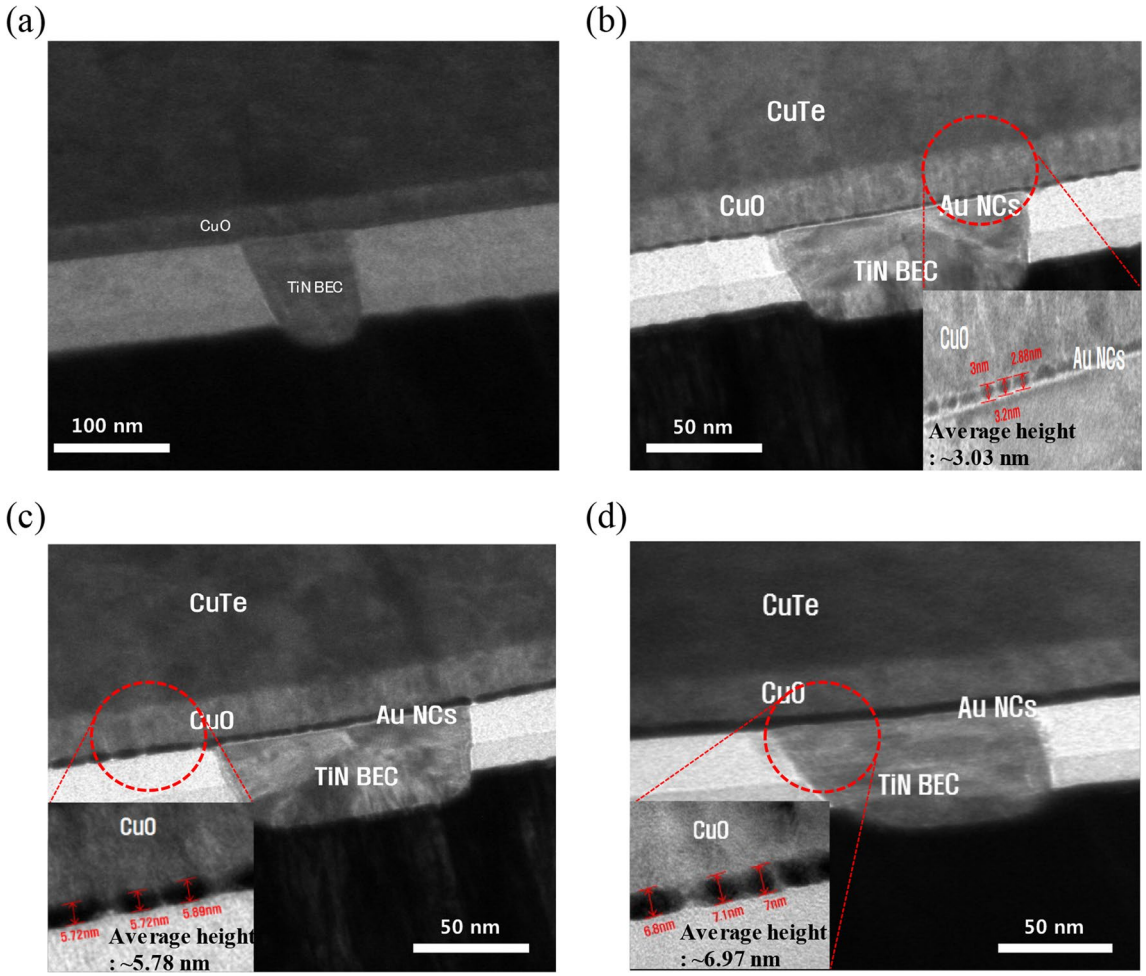


**Fig. 2** Cross-sectional TEM images of the designed CBRAM cells (**a**) without Au NCs, **b** 1 nm thick Au thin film, **c** 3 nm thick Au thin film, and **d** 5 nm thick Au thin film

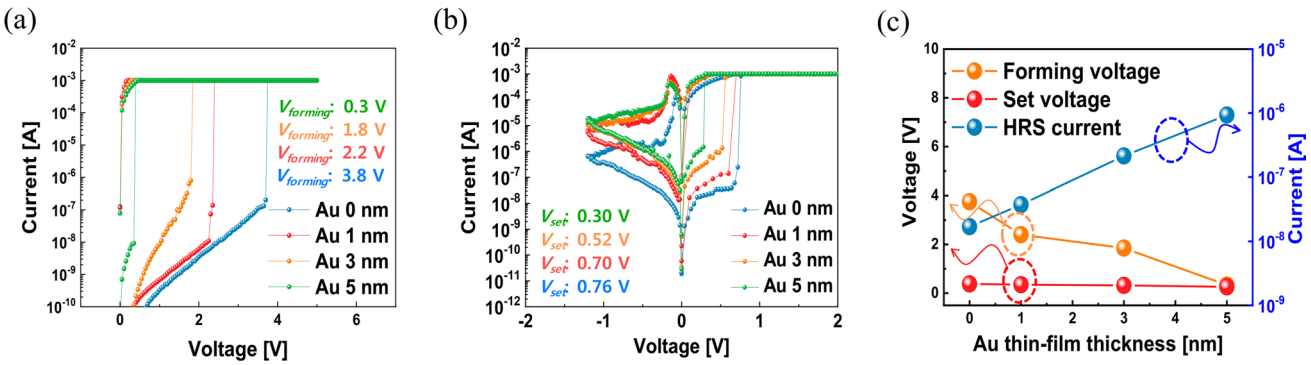


**Fig. 3** Electrical characteristics of the CBRAM cells without and with Au NCs. **a** Electroforming process of the CBRAM cells, **b** bistable resistive switching of the CBRAM cells, **c** summarized electroforming voltage, set voltage, and HRS currents depending on the thickness of the Au thin film

resistive switching measurements of the designed CBRAM cell, we demonstrated that forming-free characteristics can be achieved in the CBRAM cell by precisely controlling the size of the Au NCs in the CuO resistive switching layer and TiN bottom electrode interface.

Artificial synaptic devices require multilevel states to achieve high recognition accuracy for training and testing artificial neural networks (ANNs). Most CBRAM cells have multilevel states by control the degree of formation and rupture of conductive metal filaments in the resistive switching layer. To investigate the multi-level states of the designed CBRAM cell with the Au thin film of thickness 5 nm, DC I-V measurements were conducted by varying the compliance current level from $10^{-5}$ to $10^{-3}$ A, as shown in Fig. 4a. Typically, the LRS current level increases with the compliance current level. Thus, by controlling the compliance current level, our designed CBRAM cell with an Au thin film of 5 nm thickness could attain four level states (i.e., $I_{off}$, $I_{int2}$, $I_{int1}$, and $I_{on}$). It may be noted that the applied reset voltage was − 1.2 V at all compliance current levels. Additionally, we performed an endurance test for the four-level states, as shown in Fig. 4b. The designed CBRAM cell embedded with Au NCs exhibited a high endurance of $10^5$ cycles in multilevel states. The currents were read at 0.1 V. Furthermore, the CBRAM cell had a high retention time of $10^5$ s for the multilevel states, as shown in Fig. 4c. The highly reliable electrical characteristics of the designed CBRAM cell embedded with Au NCs (i.e., Au thin film of 5 nm) are due to the forming-free characteristics achieved by precisely controlling the size of the Au NCs.

Based on these multilevel states in the DC I–V characteristics, the LTP and LTD characteristics were evaluated during consecutive pulse operations, as shown in Fig. 5. As neuromorphic chips are typically trained and tested in pulse operations, the synaptic modulation of artificial synaptic devices should be tested under consecutive stimulus conditions (i.e., voltage pulses), unlike DC I–V scanning. To measure the synaptic modulation of the CBRAM cell without Au NCs, 128 voltage pulses with an amplitude of 0.78 V for potentiation and 128 voltage pulses with an amplitude of − 0.20 V for depression were sequentially applied to the CBRAM cell for 20 cycles, as shown in Fig. 5a. The read voltage pulses of amplitude 0.20 V were applied between consecutive voltage pulses to output the conductance of the CBRAM cell without Au NCs. In addition, the widths of the voltage pulses for potentiation, depression, and read operations were 5 ms, and the interval between consecutive voltage pulses was also 5 ms. Consequently, the synaptic modulation characteristics of the CBRAM cell without Au NCs presented a large variation under continuously applied voltage conditions. In practice, such a large variation in synaptic modulation is unsuitable for training and testing ANNs. However, the variation in synaptic modulation in the consecutive voltage pulse condition is drastically reduced with increasing thickness of the Au thin film in the case of the CBRAM cell embedded with Au thin films of thickness 1, 3, and 5 nm in Fig. 5b–d. In particular, the synaptic modulation of the designed CBRAM cell with 5 nm thick Au thin film exhibits stable operation under consecutive stimulus conditions. It may be noted that the amplitudes of the voltage pulses for potentiation in the CBRAM cells with Au thin films of thicknesses 1, 3, and 5 nm are 0.72 V, 0.55 V, and 0.32 V, respectively. In Fig. 5e–h, we mathematically calculated the synaptic variation of the maximum conductance values for 20 cycles in the CBRAM cells without Au NCs and with Au thin films of thicknesses 1, 3, and 5 nm. In the CBRAM cell without Au NCs, the mean and standard deviation of the maximum conductance values are 5.24 ms and 1.08 ms, respectively, and the coefficient of variation is 20.61%, as shown in Fig. 5e. In addition, the mean and standard deviation of the maximum conductance values are 5.25 ms and 0.60 ms, respectively, and the coefficient of variation is 11.43% for the CBRAM cell with Au thin film of 1 nm thickness, as shown in Fig. 5f. Moreover, in the case of the CBRAM cells with Au thin films of 3 and 5 nm thicknesses, the mean values of the

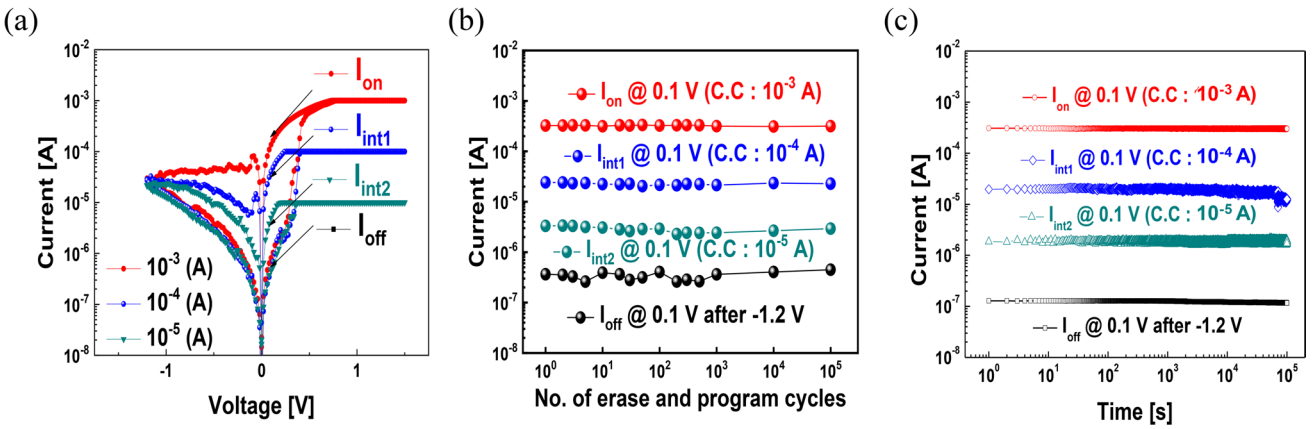


**Fig. 4** Multilevel switching of the CBRAM cells with 5-nm thick Au thin film. **a** Multilevel switching of the designed CBRAM cell by varying the compliance current level, **b** write/erase endurance cycles, and **c** retention time for multilevel characteristics

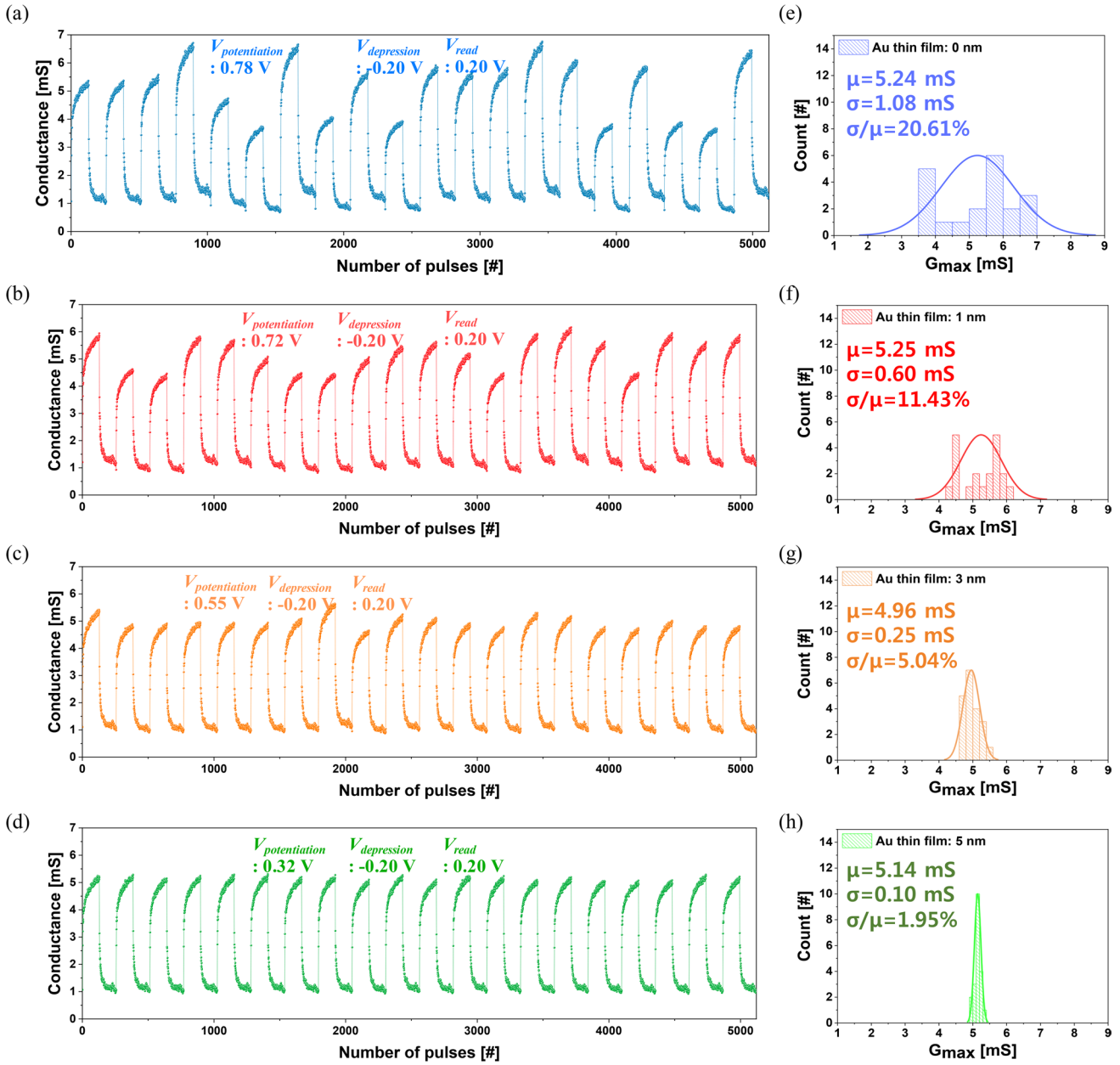


**Fig. 5** Synaptic modulation of the CBRAM cell without **a** Au NCs and embedded with Au thin film of thickness **b** 1 nm, **c** 3 nm, and **d** 5 nm, respectively. Synaptic variations in the CBRAM cell without **a** Au NCs and embedded with Au thin films of thickness **b** 1 nm, **c** 3 nm, and **d** 5 nm, respectively, represented by histograms

maximum conductance values are 4.96 ms and 5.14 ms, and the standard deviations of the maximum conductance values are 0.25 ms and 0.10 ms, respectively. Thus, the coefficient of variation for the CBRAM cell with Au thin film of 5 nm thickness is remarkably improved up to 1.95%, as shown in Fig. 5h. These results imply that the highly improved variation in the LTP and LTD characteristics of the designed CBRAM cell with Au thin film of 5 nm thickness is achieved through forming-free characteristics. Finally, we performed a hardware-based DNN simulation and evaluated the test accuracy of the image recognition depending on variations in synaptic modulation, as shown in Fig. 5.

To perform a hardware-based DNN simulation using variations in synaptic modulation, a DNN with 784 input neurons, 128 hidden neurons, and 10 output neurons was designed, as shown in Fig. 6a. The designed DNN was trained using a modified handwritten image dataset from the National Institute of Standards and Technology

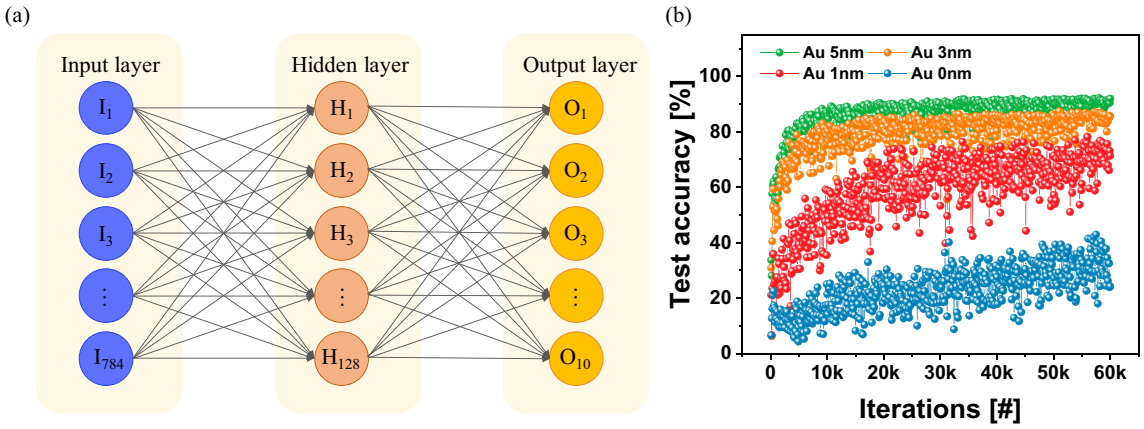


**Fig. 6** Hardware-based DNN simulation. **a** Structure of the designed DNN, and **b** test accuracy for 10,000 MNIST hand-written images depending on the Au thin film in the designed CBRAM cells

(MNIST). The MNIST dataset consists of 60,000 image data for training and 10,000 image data for testing. Moreover, each handwritten image is a 28 × 28-pixel matrix with 8-bit intensity (i.e., 0–255). In the training process, the MNIST image data with a 28 × 28-pixel matrix were converted to a 784 × 1 vector using the flattening method and input to the designed DNN. Subsequently, the weighted summation process between the input and hidden layers was conducted using the input MNIST image data and the synaptic weights of the designed CBRAM cell with 5-nm thick Au thin film. The weighted summation values were then input to the next layer of hidden neurons and converted to an activation signal using the rectified linear unit (ReLU) function of the hidden neurons. Subsequently, the weighted summation process between the hidden and output layers was again performed using the input activation signal and synaptic weights. The weighted summation values between the hidden and output layers were input to the next layer of output neurons, and the output signals were generated using the softmax function of the output neurons. The errors between the generated output signals and one-hot encoded targets (i.e., the labels of the training image dataset) were calculated as sign functions for training hardware-based DNN simulations. The backpropagation algorithm for training the hardware-based DNN was based on a previously reported study [31]. The discrete and limited conductance levels of the designed artificial synaptic device were used in the weight update process. Moreover, we applied variations in synaptic modulation in CBRAM cells without Au NCs and with Au thin films of thicknesses 1, 3, and 5 nm in the training process of the designed DNN. The variation in synaptic modulation in the hardware-based DNN was applied to the weight update process as follows [32].

$$\Delta G_{\text{real}} = \Delta G_{\text{expected}} \times (1 + k)\left(k \le \pm\frac{\sigma}{\mu}\right)$$

Here, $\sigma$ and $\mu$ denote the standard deviation and mean value of conductance, respectively. In the case of the CBRAM cell without Au NCs, the test accuracy for 10,000 test images is less than ~ 40% over 60,000 iterations (i.e., 60,000 training images), as shown in Fig. 6b. This test accuracy indicates that a CBRAM cell without Au NCs cannot be employed as an artificial synaptic device because of high variation in synaptic modulation. However, the final test accuracy is abruptly increased up to 91.95% when the thickness of the Au thin film is increased from 1 to 5 nm. This result is due to the variation in synaptic modulation of the designed CBRAM cell, which is dramatically improved from 20.61 to 1.95% by inserting Au NCs in the CuO resistive switching layer and TiN bottom electrode interface. Thus, the designed CBRAM cell embedded with an Au thin film of thickness 5 nm can be employed as a highly reliable artificial synaptic device to improve the online training and test accuracy of advanced neuromorphic computing architectures.

## 3 Conclusion

In summary, a highly reliable CBRAM cell embedded with Au NCs with forming-free characteristics has been designed, and its applicability as an artificial synaptic device has been demonstrated. Forming-free characteristics could be achieved by precisely controlling the thickness of the inserted Au thin film in the CuO resistive switching layer and TiN bottom electrode. In addition, the CBRAM cell with Au thin film of 5-nm thickness exhibits multilevel current states depending on the compliance current level.

In neuromorphic applications, the variation in synaptic modulation of the CBRAM cell with Au thin film of 5-nm thickness is remarkably reduced up to 1.95%. Finally, the test accuracy for 10,000 MNIST test images was drastically improved to 91.95% after 60,000 iterations. These findings can contribute to the development of highly reliable synaptic devices within the hyper-scale synaptic cores of neuromorphic chips.

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